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Editorial

Thin Film Applications in Advanced Electron Devices

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The application of thin films has always been a very important subject for the semiconductor industry and the scientific community. This is especially true for metal-oxide-semiconductor field effect transistor (MOSFET) technology in integrated circuits (ICs). The concept of MOSFET is based on the modulation of channel carriers by an applied gate voltage across a dielectric thin film. The electric charges in dielectrics will respond to an applied electric field through the change of dielectric polarization. The conduction current in dielectric films at normal applied electric field will be very small because their conductivities are inherently very low. However, the conduction current through the dielectric films is considerable when a relatively large electric field is applied. This considerable conduction current is owing to many different conduction mechanisms, which is crucial to the successful applications of dielectric thin films.

In general, there are two types of conduction mechanisms in dielectric films, that is, electrode-limited conduction mechanism and bulk-limited conduction mechanism [1]. The electrode-limited conduction mechanism relies on the electrical properties at the electrode-dielectric interface. Based on this type of conduction mechanism, the key physical properties are the barrier height at the electrode-dielectric interface and the effective mass of the conduction carriers in dielectric films [1]. Meanwhile, the bulk-limited conduction mechanism relies on the electrical properties of the dielectric itself. Based on the bulk-limited conduction mechanisms, some important physical parameters in the dielectric films can be obtained, such as the trap level, the trap spacing, the trap density, the carrier drift mobility, the dielectric relaxation time, and the density of states in the conduction band [1]. One can find a review article in which the analytical methods of conduction mechanisms in dielectric films are discussed in detail [1]. Aside from the conduction mechanisms, the interface properties between silicon channel and gate dielectric are critical to the performance and reliability of MOSFETs. The methods for the characterization of electrical properties at the dielectric/Si interface can be performed by several techniques, for example, capacitance-voltage method, charge pumping method, gate-diode method, and subthreshold swing measurement [2, 3]. Based on these techniques, the surface state capture cross section at the interface between silicon and gate dielectric can be obtained. The quality of interface between silicon and dielectric film is associated with the successful applications of dielectric thin films in semiconductor industry.

Recently, the developments of next generation nonvolatile memory (NVM) devices are required because the physical limitations of traditional flash memory devices are approaching [4]. A variety of thin films have been studied for the application of NVM devices. For example, $BiFeO_3$ film is antiferromagnetic at room temperature, and it is promising for the applications of magnetic random access memory (MRAM) and spintronic devices [5]. Moreover, lead-zirconium-titanate (PZT) film is suitable for building the ferroelectric random access memory (FRAM) because of its ferroelectricity [6]. Recently, the resistance random access memory (RRAM) device has attracted a great deal of attention for the next generation NVM applications [7]. Since the RRAM technology is well compatible with

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the CMOS process, the scaling of RRAM devices may keep on in terms of the low power operation. This benefit will bring a strong cost-competitiveness to RRAM. Additionally, the advantages of RRAM include small cell size, simple cell structure, high switching speed, high operation durability, multistate switching, and three-dimensional architecture. The resistance switching behavior has been reported for a variety of materials such as binary metal oxides, solid-state electrolytes, organic compounds, amorphous Si, and perovskite-type oxides [4, 7]. All these materials mentioned above were made by thin films for the applications of advanced electron devices, for example, MRAM, FRAM, and RRAM. Recently, the applications of organic electronics were attractive due to the advantages of low cost, light weight, large-area manufacturing, and mechanical flexibility. Thus, the organic thin films were proposed and implemented for the applications of organic thin film transistors, solar cells, organic light-emitting diodes, and sensors.

In addition to the dielectric thin films used by the fabrication of advanced electron devices, the metallic thin films used by the interconnection between devices are also required to be considered. In deep-submicron CMOS technology, Cu thin film has been used as an interconnect metallization material to reduce the effect of the resistance capacitance (RC) delay because of its lower resistivity and higher electromigration (EM) resistance [8]. Aside from the interconnection application, the metallic thin films can be used in the fabrication of electron devices, such as the ferromagnetic films used in MRAM devices.

We hope that readers will realize in this special issue not only the thin film applications in advanced electron devices, but also the characterization methods for the electrical properties in thin films and their related interface, such as the interface barrier height, the carrier effective mass, the trap energy level, the trap spacing, the trap density, the dielectric relaxation time, and the density of states in the conduction band, among others.

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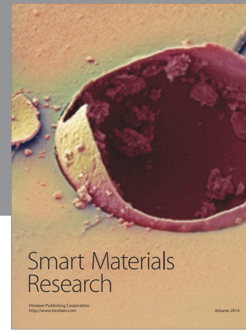

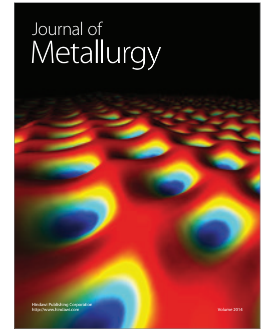

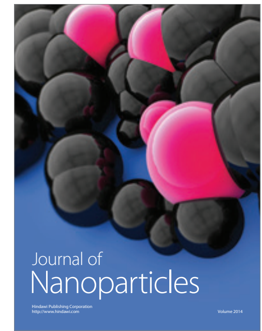

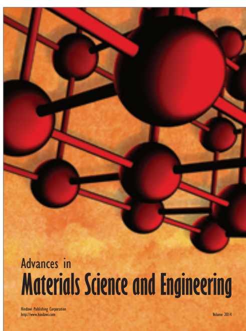

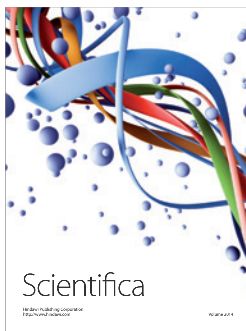

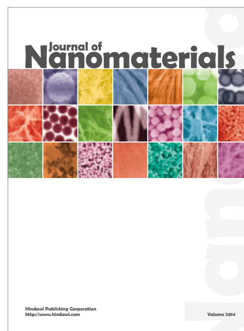

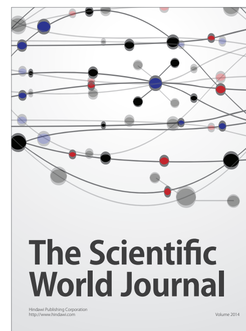

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